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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,767	01/23/2002	Tieer Gu	8733.215.20	7130

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MCKENNA LONG & ALDRIDGE LLP  
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EXAMINER
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DOLAN, JENNIFER M

ART UNIT	PAPER NUMBER
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2813

DATE MAILED: 03/04/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/052,767

Applicant(s)

GU ET AL. 

Examiner

Jennifer M. Dolan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                  | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). ____.  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>2</u> . | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Double Patenting*

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 5,920,084 to Gu et al. Although the conflicting claims are not identical, they are not patentably distinct from each other because the sub-genus in the '084 patent, wherein the insulating layer is "at least about 1.5 microns thick" anticipates the genus in the present application, wherein the insulating layer can be of any thickness, and thus a patent to the genus would extend the rights of the sub-genus should the genus issue as a patent.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

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having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,003,356 to Wakai et al. (cited by applicant) in view of U.S. Patent No. 5,591,676 to Hughes et al. (cited by applicant).

Wakai discloses a liquid crystal display with a large pixel aperture ratio (column 7, lines 1-10) comprising: a liquid crystal layer (117) sandwiched between first (112) and second (116) substrates (figure 5); an array of thin film transistors (figures 5, 9, and 13) and corresponding pixel electrodes (110) mounted on the first substrate (figure 13), each of the thin film transistors including a semiconductor layer (104), a gate electrode (102) connected to a gate address line (figure 9); a drain electrode (106) connected to a drain address line (figure 9), and a source electrode (107) connected to one of the corresponding pixel electrodes (figure 13), and wherein the pixel electrode connected to the source electrode overlaps the gate and drain address lines over longitudinal edges thereof (figure 9; column 8, lines 31-44); and a substantially continuous insulating layer (108) disposed between the pixel electrode and the address lines (figure 13). It is implicit that Wakai discloses that the insulating layer has sufficient thickness so as to reduce capacitive cross-talk in the display by reducing the pixel electrode-address line parasitic capacitance  $C_{pl}$  in the areas of overlap, because Wakai states that the capacitance resulting from the pixel electrode and gate overlap is sufficiently small (see column 12, lines 22-40). Wakai further discloses that the insulating layer is made of polyimide (column 5, lines 49-54), which is known in the art to have a dielectric constant of about 2.8-3.5 (see Hughes, column 1, lines 25-27 for typical dielectric constant values for polyimide).

Wakai fails to specifically point out that the dielectric constant is less than 3.0.

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Hughes teaches the use of low dielectric constant materials as passivation and insulating layers for transistor devices (column 2, lines 36-54, column 3, lines 54-58). Hughes additionally teaches that low dielectric constant materials are desirable for separating adjacent conductive lines in transistors, in order to avoid large capacitive loads which degrade transistor performance (column 1, lines 26-29), and to allow for shrinking of devices without adversely affecting device performance (column 1, lines 29-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the insulating layer of Wakai has a dielectric constant of less than 3.0, as suggested by Hughes. The rationale is as follows: A person having ordinary skill in the art would have been motivated to specify that the insulating layer has a low dielectric constant, because Wakai teaches that it is desirable to minimize the capacitance between the pixel electrode and gate line (Wakai, see column 12, lines 22-40), and Hughes teaches that by decreasing the dielectric constant between adjacent conductive lines in a transistor, the capacitive load is minimized (Hughes, column 1, lines 13-32). Because Wakai discloses that the insulating layer is polyimide, which typically has a dielectric constant between 2.8 and 3.5, it is well within the purview of a person having ordinary skill in the art to select polyimides with a dielectric constant in the range of 2.8 to 3.0, in order to reduce the parasitic capacitance between the gate line and pixel electrode.

### ***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure

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U.S. Patent No. 5,463,483 to Yamazaki and U.S. Patent No. 5,734,455 to Yoshida et al. disclose LCD pixels using auxiliary capacitors to decrease the effect of parasitic capacitance between the gate and pixel electrodes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (703) 305-3233. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jennifer M. Dolan  
Examiner  
Art Unit 2813

jmd  
February 28, 2003

  
**CARL WHITEHEAD, JR.**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**